National Aeronautics and Space Administration

NASA Electronic Parts and Packaging (NEPP) Program

http://nepp.nasa.gov

Kenneth A. LaBel
and Michael J. Sampson
Co-Managers NEPP Program

NEPP Mission

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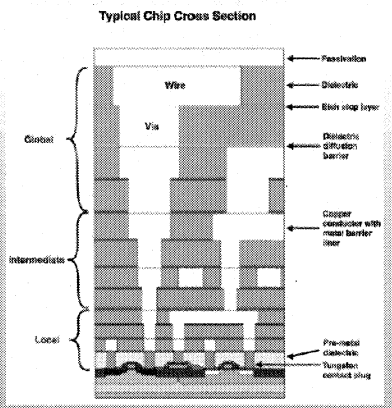

Industrial Exhibit Poster to be presented by Kenneth LaBel at several conferences throughout 2008 (including CMSE, HEART, SEESYM, NSREC, and RADEX).

NEPP Overview

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  - **7 NASA Centers and JPL actively participate**
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  - **Integrated circuits such as a processor in a computer or optical components such as might be used in a communication link.**
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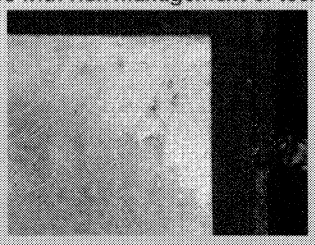
Electrical overstress failure in a commercial electronic device

- **NEPP interests span electronic parts technologies**
  - **Emerging semiconductors and packages**
  - **Commonly-used "mission building blocks"**
  - **New state-of-the-art commercial products**
- **NEPP is multi-disciplinary**
  - **Including radiation, materials, test, experimentation, process and specification experts across NASA and its partners**
- **NEPP has close, cooperative and long-standing relationships with government and non-government entities worldwide**
- ***NEPP provides unique capabilities within NASA***
  - ***Evaluate technologies in advance of mission needs***
  - ***Provide assistance with risk management of technology insertion***



NEPP Task: Packaged Device Deprocessing for Testability

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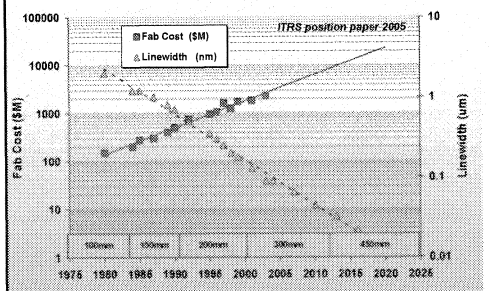
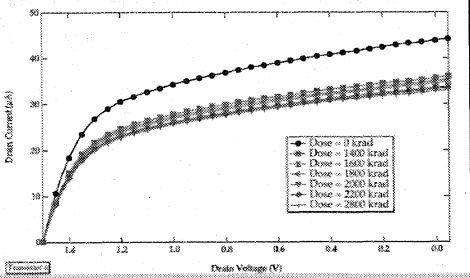
CMOS Scaling – New Challenges



Modeling, simulation, device physics understanding of failure modes, data gathering and analysis, and reliability prediction

- Foundation for technology insertion of the next generation of scaled microelectronics.

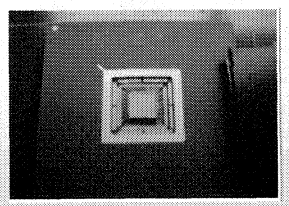
CMOS Scaling Reliability
NEPP POC: Mark White, JPL



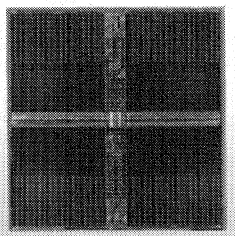
Sample CMOS Scaling 90nm Transistor Test

CMOS Scaling Radiation
NEPP POC: Ken LaBel, GSFC

Sample NEPP Technology Areas

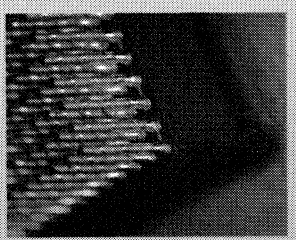


Leveraging
Rad-Hard by Design (RHBD) Efforts

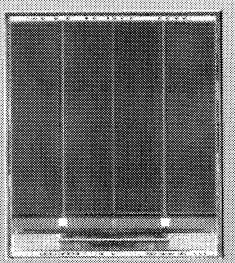


SDRAM

Evaluating state-of-the-art memory



Advanced Electronics Packaging



Flash

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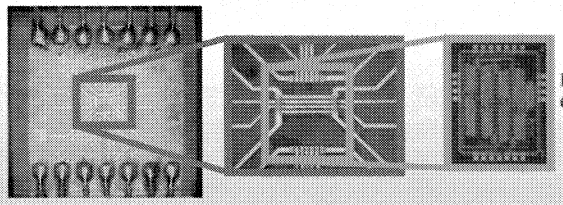
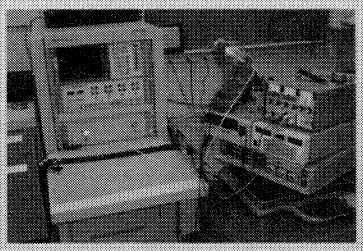
Sample Efforts on Advanced Electronic Technologies

Low and high magnification photographs of embedded OpAmp assemblies



Photograph of Quad OpAmp

NEPP POC for embedded actives: Linda Del Castillo, JPL



SiGe RF Extreme Temperature Test Set

NEPP POC for extreme temperature: Richard Patterson, GRC

Improving understanding of risk and test methods

Can we test anything completely?

"Complete" Single Event Effect (SEE) Radiation Test Matrix for a commercial SDRAM (does not include temperature variations)

3	Number of Samples
68	Modes of Operation
4	Test Patterns
3	Frequencies of Operation
3	Power Supply Voltages
3	Ions
3	Hours per Ion per Test Matrix Point

66096 Hours
2754 Days
7.54 Years

Implications:

- Test planning and performance is now application-specific focused
- Existing datasets must be viewed in the same light (application)

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NEPP and FPGAs-
A Sampling of Challenges

Can we "qualify" the system without breaking the bank?

New Connectors
-higher-speed, lower noise
-serial/parallel

New Silicon
-90nm CMOS
-new materials

New Board Material
-thermal coefficients
-material interfaces

New Architectures
-new interconnects
-new power distribution
-new frequencies

New Workmanship
-inspection, lead free
-stacking, double-sided
-signal integrity

New Design Flows/Tools
-programming algorithms, application
-design rules, tools, simulation, layout
-hard/soft IP instantiation

New Package
-Inspection
-Lead free

FPGA Insertion Processes: Viewed as a System

FPGA Insertion Process

Foundry	Vendor	User
Technology	Design	Application
Yield	Test	Design process
Quality Program	Quality Program	Screening

Successful insertion requires significant contributions from all three areas.

NEPP POC:
Doug Sheldon, JPL

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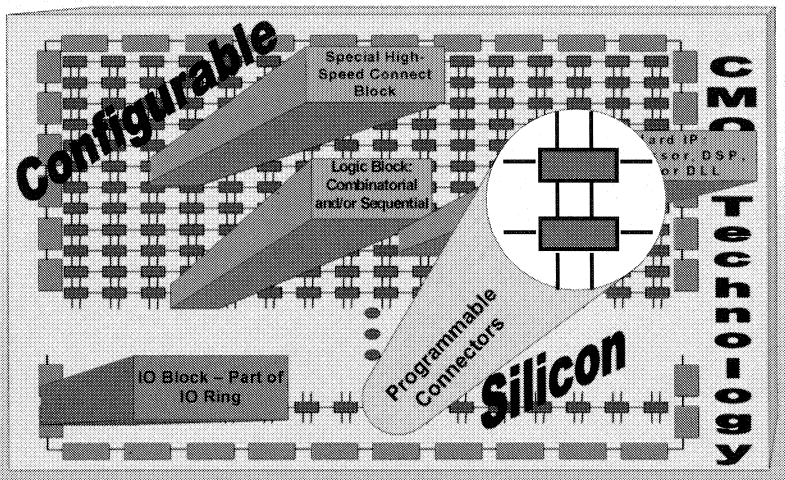
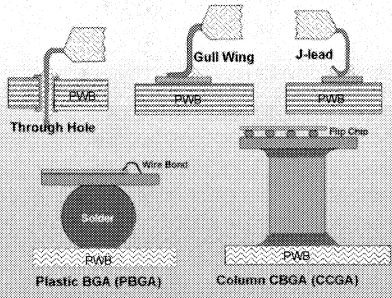
FPGAs: Radiation Testing, Test Method Development, Data Interpretation and User Insertion

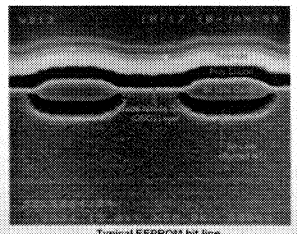


NEPP POCs:
Melanie Berg, MEI/GSFC
Greg Allen, JPL

FPGAs: Packaging and Support Devices

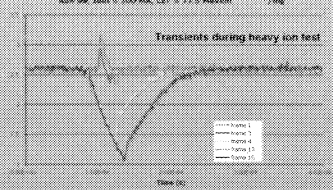


Device Packaging
NEPP POCs: Reza Ghaffarian, JPL
Jill Mohammed, GSFC



Typical EEPROM bit line
http://www.eetimes.com/editorial/2000/applications0012.html

Radiation and Reliability of FLASH NVMs
NEPP POCs: Doug Sheldon, JPL (reliability)
Tim Oldham, PerotSystems/GSFC (radiation)



Radiation Effects on Low-Voltage Regulators
NEPP POC: Ken LaBel, GSFC (acting)

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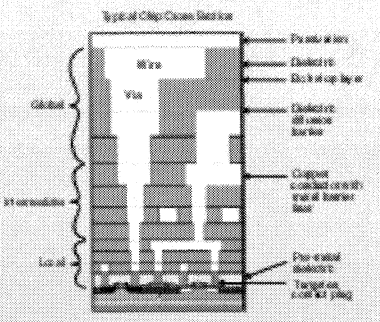

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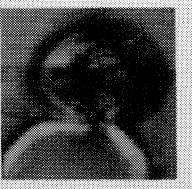

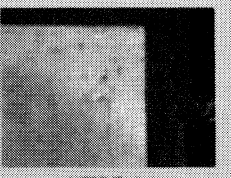

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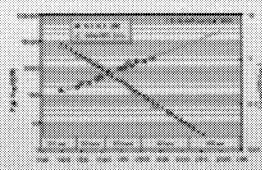

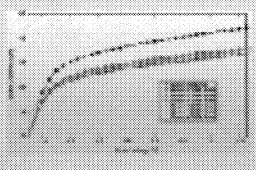

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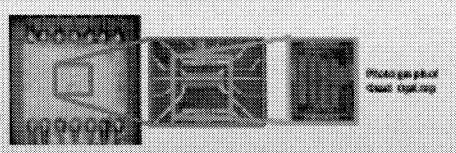

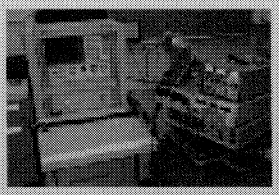

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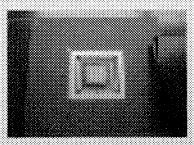

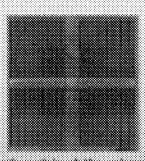

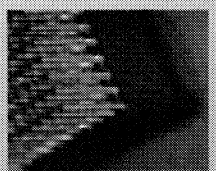

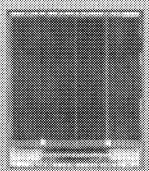

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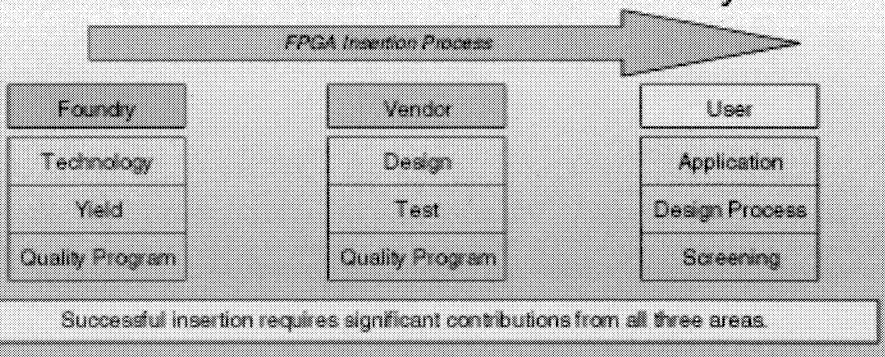

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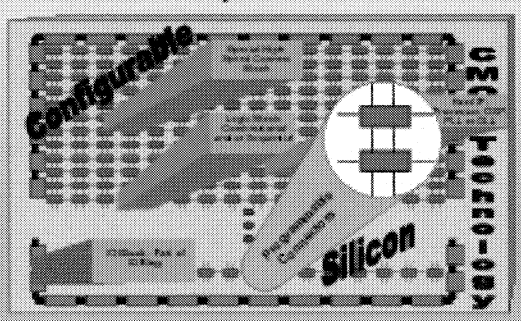
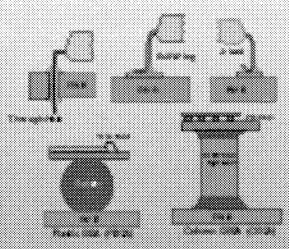
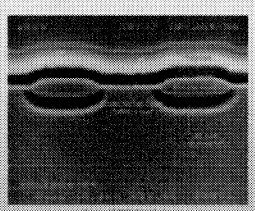
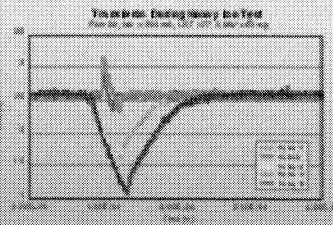


FPGAs: Packaging and Support Devices







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